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WINSTEAD SECHREST & MINICK P.C.
P.O. BOX 50784
DALLAS, TX 75201

| EXAMINER | |
|---|---|
| PARIHAR, SUCHIN | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/790,381 | LUKANC ET AL. |
| | Examiner | Art Unit |
| | Suchin Parihar | 2825 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21 and 24-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13,15,17-21 and 24-27* is/are rejected.

7)☒ Claim(s) *12,14 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application 10/790,381, arguments filed 2/2/2007. Claims 1-21 and 24-27 are pending in this application. Claims 22-23 are cancelled.

2. Applicant's arguments filed 2/2/2007 have been fully considered but they are not persuasive. The applicable rejections from the previous office action are incorporated herein.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-3, 8, 9, 13, 15, 17-21 and 27 are rejected under 35 U.S.C. 102(e)** as being anticipated by Kroyan et al. (PG Pub 2005/0188338).

5. With respect to claim 1, Kroyan teaches: (a) generating an initial layout representation in accordance with a plurality of design rules (i.e. baseline design rule which is used in the physical layout generation process, pg 4, paragraph [0051]); (b) simulating how structures within at least a portion of the initial layout will pattern on a

wafer (i.e. simulation engine which predicts the layout pattern generation on a wafer, pg 5, paragraph [0075]); (c) based on the simulating step, identifying portions of the layout representation which include structures demonstrating poor manufacturability (i.e. portions of the design that have a poor manufacturability, pg 2, paragraph [0021]); (d) based on the simulating step, identifying portions of the layout representation in which extra manufacturability margin is present (i.e. pattern types with excess manufacturability margin, pg 3, paragraph [0046]); and (e) modifying (i.e. using a layout modification engine, pg 6, paragraph [0081]) at least one of: (i) portions of the layout representation which include structures demonstrating poor manufacturability (i.e. modifying manufacturability weak spots, pg 6, paragraph [0081]) and (ii) portions of the layout representation in which extra manufacturability margin is present.

6. With respect to claim 27, Kroyan teaches

defining a manufacturability figure of merit (FOM) (i.e. discussion of aerial image metrics such as: intensity, image slope, image log-slope that contain pattern printability information, pg 6, paragraph [0076], which may serve to provide an FOM, as described on page 13 of Applicants' specification);

simulating how the layout will pattern on a wafer (i.e. simulation engine which predicts the layout pattern generation on a wafer, pg 5, paragraph [0075]);

evaluating manufacturability of portions of the layout based on the manufacturability FOM (i.e. pass module 5107 which determines whether manufacturability parameters are out of tolerance, pg 6, paragraph [0079]);

based on the evaluating step, modifying the design rule compliant layout (i.e. layout modification engine optimizes weak spots –those spots that are out of tolerance, pg 6, paragraph [0081]); and

wherein modifying the design rule compliant layout includes modifying the layout in violation of at least one design rule with which the layout is compliant (i.e. layout modification due to non-compliance properties of layout patterns, pg 6, paragraph [0080]).

7. With respect to claim 2, Kroyan teaches all the elements of claim 1, from which the claim depends. Kroyan teaches: (f) simulating how structures within at least a portion of the modified layout representation will pattern on a wafer (i.e. after layout modification, layout may be routed back to simulation engine, wherein simulation engine simulates patterns on a wafer, pg 6, paragraph [0082]); and (g) repeating steps (c)-(f) until no portions of the layout representation demonstrate poor manufacturability (i.e. steps may continue iteratively until no manufacturing weak spots remain, pg 6, paragraph [0082]).

8. With respect to claim 3, Kroyan teaches all the elements of claim 1, from which the claim depends. Kroyan teaches: performing at least one optical proximity correction (OPC) on the initial layout representation before step (b) (i.e. layout manipulation by OPC, pg 4, paragraph [0063]).

9. With respect to claim 8, Kroyan teaches all the elements of claim 1, from which the claim depends. Kroyan teaches: defining a manufacturability figure of merit (FOM) (i.e. discussion of aerial image metrics such as: intensity, image slope, image log-slope

that contain pattern printability information, pg 6, paragraph [0076], which may serve to provide an FOM, as described on page 13 of Applicants' specification); and evaluating the manufacturability of at least a portion of the simulated layout representation based on the manufacturability FOM (i.e. pass module 5107 which determines whether manufacturability parameters are out of tolerance, pg 6, paragraph [0079]).

10. With respect to claim 9, Kroyan teaches all the elements of claim 8, from which the claim depends. Kroyan teaches: identifying one or more metrics (i.e. image log slope, intensity, image contrast, pg 6, paragraph [0076]) which are indicative of a manufacturable layout representation; and selecting acceptable ranges for the one or more metrics (i.e. determining the best values of these [metric] tolerances, pg 6, paragraph [0076]).

11. With respect to claim 13, Kroyan teaches all the elements of claim 1, from which the claim depends. Kroyan teaches: identifying metrics (i.e. image log slope, intensity, image contrast, pg 6, paragraph [0076]) which are indicative of a manufacturable layout representation.

12. With respect to claim 15, Kroyan teaches all the elements of claim 1, from which the claim depends. Kroyan teaches: wherein for portions of the layout representation in which extra manufacturability margin is present, step (e) includes compacting at least a portion of the layout representation (i.e. for pattern types with excess manufacturability margin, it may be possible to tighten or compact the design, pg 3, paragraph [0046]).

13. With respect to claim 17, Kroyan teaches all the elements of claim 1, from which the claim depends. Kroyan teaches: wherein step (b) includes at least one of resolution

enhancement technologies (RET), optical proximity correction (OPC), proximity to other structures, density of structures and corner rounding (layout manipulation including a discussion of OPC and RET, pg 4, paragraph [0063]).

14. With respect to claim 18, Kroyan teaches all the elements of claim 1, from which the claim depends. Kroyan teaches: wherein step (e) includes violating at least one of the plurality of design rules (i.e. discussion of design rule violation types, pg 6, paragraph [0079]).

15. With respect to claim 19, Kroyan teaches all the elements of claim 1, from which the claim depends. Kroyan teaches: wherein step (e) is performed despite there existing no violation of any of the plurality of design rules (i.e. layout may be compacted [or modified] due to excess manufacturability margin, wherein modification is not a result of a violation of a design rule, pg 5, paragraph [0046]).

16. With respect to claim 20, Kroyan teaches all the elements of claim 1, from which the claim depends. Kroyan teaches: wherein step (c) includes providing a graphical representation (i.e. geometrical configuration of the layout, pg 6, paragraph [0087]) indicating structures demonstrating poor manufacturability (non-compliant manufacturability parameters, pg 6, paragraph [0086]).

17. With respect to claim 21, Kroyan teaches all the elements of claim 20, from which the claim depends. Kroyan teaches: wherein step (d) includes providing a graphical representation (i.e. geometrical configuration of the layout, pg 6, paragraph [0087]) identifying portions of the layout representation in which extra manufacturability (i.e spacing, gaps, pitch and the like, pg 6, paragraph [0087]) margin is present.

## *Claim Rejections - 35 USC § 103*

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. **Claim 4-7, 10-11 and 24-26 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Kroyan et al (PG Pub 2005/0188338) in view of Anderson et al. (6,425,113).

20. With respect to claim 24, Kroyan teaches:

defining a manufacturability figure of merit (FOM) (i.e. discussion of aerial image metrics such as: intensity, image slope, image log-slope that contain pattern printability information, pg 6, paragraph [0076], which may serve to provide an FOM, as described on page 13 of Applicants' specification);

simulating how the layout will pattern on a wafer (i.e. simulation engine which predicts the layout pattern generation on a wafer, pg 5, paragraph [0075]);

evaluating manufacturability of portions of the layout based on the manufacturability FOM (i.e. pass module 5107 which determines whether manufacturability parameters are out of tolerance, pg 6, paragraph [0079]);

based on the evaluating step, modifying the design rule compliant layout (i.e. layout modification engine optimizes weak spots –those spots that are out of tolerance, pg 6, paragraph [0081]);

identifying one or more metrics (i.e. image log slope, intensity, image contrast, pg 6, paragraph [0076]) which are indicative of a manufacturable layout representation; and

selecting acceptable ranges for the one or more metrics (i.e. determining the best values of these [metric] tolerances, pg 6, paragraph [0076]).

Kroyan fails to teach: wherein the evaluating step includes: performing optical rule checking (ORC) on the simulated layout using the selected acceptable ranges for the one ore more metrics.

However, Anderson teaches: wherein the evaluating step includes: performing optical rule checking (ORC) on the simulated layout (ORC component simulates the performance expected on the wafer and determines violation of tolerances, Col 7, lines 22-30) using the selected acceptable ranges for the one or more metrics (see metrics cited in Kroyan).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Anderson into the invention of Kroyan for the following reason(s): Anderson would improve the invention of Kroyan by providing an ORC component whose job is to determine whether the applied OPC in Kroyan will have the desired corrective effect on the final layout (see Anderson, Col 2, lines 50-55).

21. With respect to claim 4, Kroyan teaches all the elements of claim 1, from which the claim depends. Kroyan fails to teach: wherein step (c) includes performing optical rule checking (ORC) on the simulated layout representation. However, Anderson teaches: wherein step (c) includes performing optical rule checking (ORC) on the simulated layout representation (ORC component simulates the performance expected on the wafer and determines violation of tolerances, Col 7, lines 22-30). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Anderson into the invention of Kroyan for the following reason(s): Anderson would improve the invention of Kroyan by providing an ORC component whose job is to determine whether the applied OPC in Kroyan will have the desired corrective effect (see Anderson, Col 2, lines 50-55).

22. With respect to claim 5, Kroyan in view of Anderson teaches all the elements of claim 4, from which the claim depends. Kroyan teaches: checking at least one of aerial image metrics (i.e. evaluation [checking] of image log slope & intensity, pg 6, paragraph [0076]), resist image metrics and post exposure bake metrics. Examiner notes that on page 13 of Applicant's specification, intensity and logarithm of slope are defined as aerial image metrics.

23. With respect to claims 6 and 25, Kroyan in view of Anderson teaches all the elements of claims 5 and 24, from which the claims depend respectively. Kroyan teaches a simulated layout representation over a process window (i.e. process window PW, paragraph [0076]) of focus and intensity (i.e. depth of focus DOF and intensity, paragraph[0076]). Kroyan fails to teach: performing ORC. However, Anderson

teaches: performing ORC (ORC component simulates the performance expected on the wafer and determines violation of tolerances, Col 7, lines 22-30).

24. With respect to claims 7 and 26, Kroyan in view of Anderson teaches all the elements of claims 5 and 24, from which the claims depend respectively. Kroyan teaches: wherein the aerial image metrics include at least one of image edge slope, image edge log slope, contrast (pg 6, paragraph [0076]), minimum intensity, maximum intensity, edge placement error and intensity at a given distance (i.e. image slope, image log-slope, image contrast, pg 6, paragraph [0076]).

25. With respect to claim 10, Kroyan teaches all the elements of claim 9, from which the claim depends. Kroyan fails to teach ORC. However, Anderson teaches ORC (ORC component simulates the performance expected on the wafer and determines violation of tolerances, Col 7, lines 22-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Anderson into the invention of Kroyan for the following reason(s): Anderson would improve the invention of Kroyan by providing an ORC component whose job is to determine whether the applied OPC in Kroyan will have the desired corrective effect (see Anderson, Col 2, lines 50-55).

26. With respect to claim 11, Kroyan in view of Anderson teaches all the elements of claim 11, from which the claim depends. Kroyan teaches: wherein the aerial image metrics include at least one of image edge slope, image edge log slope, contrast (pg 6, paragraph [0076]), minimum intensity, maximum intensity, edge placement error and

intensity at a given distance (i.e. image slope, image log-slope, image contrast, pg 6, paragraph [0076]).

### *Allowable Subject Matter*

27. Claims 12, 14 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

28. The following is a statement of reasons for the indication of allowable subject matter:

29. With respect to claim 12, the prior art made of record fails to teach:

selecting an exemplary layout;

generating a simulation image corresponding to how the selected exemplary layout pattern will pattern on a wafer;

evaluating a scanning electron microscope (SEM) image of the selected exemplary layout portion printed on a wafer;

identifying areas on the SEM image that are problematic with respect to manufacturability; and

for each problematic area on the SEM image, locating the corresponding portion of the simulation image and determining acceptable ranges for the one or more metrics based on the simulation image.

30. With respect to claim 14, the prior art of record fails to teach: step (e) includes at least one of (i) providing more space between adjacent structures, (ii) decreasing

linewidth of one or more structures, and (iii) making edges of one or more structures wider.

31. With respect to claim 16, the prior art of record fails to teach: step (e) includes at least one of (i) moving outer corners of structures closer to adjacent structures, (ii) moving contacts closer to inner corners of metal lines, (iii) moving contacts closer to polysilicon end caps, (iv) reshaping active or metal layers to maintain width and space, and (v) adding side extensions to polysilicon end caps.

***Response to Arguments***

32. Applicant's remarks filed 2/2/2007 have been fully considered but they are not persuasive.

33. Applicant asserts that Examiner's motivation to combine Kroyan and Anderson is insufficient to establish a prima facie case of obviousness. Examiner disagrees with this assertion.

Examiner points out that Applicant's invention performs OPC, as evidenced from Figure 7, blocks 2007 and 2008. It is well known in the art that certain verification methods are used to validate the correctness of such processes, such as Optical Proximity Correction (OPC). Anderson suggests that data generated by the OPC tool is typically imported into a simulation tool (Kroyan teaches such as simulation tool, paragraph [0075]: input design layout [which is OPC corrected, see paragraph 0074] is modeled using a simulation engine) to confirm that the OPC will have the desired corrective effect on the layout (see Anderson, Col 2, lines 50-55). Anderson goes on to say, "this is sometimes called an optical and process rule check, or ORC. Therefore, it

would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Anderson's ORC verification process into Kroyan because Anderson's ORC process improves Kroyan's OPC by providing a way for Kroyan's OPC to check the desired corrective effect on the final layout, as suggested by Anderson. More specifically, Kroyan performs OPC but does not disclose solving the problem of making sure the OPC check has the corrective effect desired by such an OPC process, wherein such effects involve modifying or manipulating process variables such as focus and intensity [i.e. aerial image metrics] over a process window as taught by Kroyan in paragraph [0076]. Kroyan describes focus and intensity as manufacturability parameters (paragraph [0076]) that are measured by a manufacturability value extractor and then compared to the manufacturability tolerance values to determine if the tolerances are met (paragraph [0078]), i.e. an OPC process. Applicant describes an ORC process with the same steps, i.e. the ORC steps as recited in the claims of Applicant's invention. Anderson provides the motivation to modify Kroyan to use the term "ORC" instead of using the description in paragraph [0035] describing "outputs from the layout processing engine [i.e. OPC process- see paragraph [0063]] are subject to verification [i.e. ORC] to ensure that processed [i.e. OPC processed] layout instances meet printability and electrical performance margins". This description results in using a OPC process verification to verify an OPC process. Anderson provides the motivation to use the term "ORC" to describe this verification process by stating, in Col 2 lines 50-55, that "The data generated by the OPC tool is then typically imported into a simulation tool, to confirm that the OPC will have the desired corrective effect". Therefore,

Anderson suggests that a process for verifying an OPC process (such as the verification described in Kroyan, paragraph [0053]) can be referred to as "ORC".

34. Applicant asserts that Kroyan fails to teach: "based on the simulating step, identifying portions of the layout representation in which extra manufacturability margin is present". Examiner disagrees with this assertion.

Examiner points out that Kroyan teaches: based on the simulating step (i.e. the output simulation results are then analyzed by a manufacturability parameter value extractor, paragraph [0076]), identifying portions of the layout representation in which extra manufacturability margin is present (i.e. there are also portions of the design that significantly exceed [i.e. extra] the minimal tolerance [i.e. margin] of the manufacturing process).

35. Applicant asserts that Kroyan fails to teach: "wherein modifying the design rule compliant layout includes modifying the layout in violation of at least one design rule with which the layout is compliant". Examiner disagrees with this assertion.

Examiner points out that Kroyan teaches: wherein modifying the design rule compliant layout (i.e. generating layout modification instructions, paragraph [0081]) includes modifying the layout in violation (non-compliance, see paragraph [0080]) of at least one design rule [DR, see Fig 10, 5111] with which the layout is compliant (i.e. no additional weak spots as per design rules, paragraph [0082 in conjunction with Fig 10]).

36. Applicant asserts that Kroyan fails to teach: "performing at least one optical proximity correction (OPC) on the initial layout representation before step (b)". Examiner disagrees with this assertion.

37. Examiner points out that Kroyan teaches: performing at least one optical proximity correction (i.e. OPC layout optimization in RET flow 2000 of Fig 6, see paragraph [0063]) on the initial layout representation before step (b) (input design layout is the output of the RET OPC flow 2000 of Fig 6; and the post-OPC input design layout is then modeled using a simulation engine in order to predict the layout pattern, paragraph [0075], i.e. prior to simulating pattern, OPC is performed on layout).

38. Applicant asserts that Kroyan fails to teach: step (e) includes: compacting at least a portion of the layout representation. Examiner disagrees with this assertion.

39. Examiner points out that Kroyan teaches: compacting at least a portion of the layout representation (i.e. for pattern types with excess manufacturability margin, it may be possible to tighten or compact the design, paragraph [0046]).

40. Applicant asserts that Kroyan fails to teach: wherein step (e) is performed despite there existing no violation of any of the plurality of design rules as recited in claim 19. Examiner disagrees with this assertion.

41. Examiner points out that paragraph [0046] of Kroyan discloses, "tighten[ing] or compact[ing] the design" for pattern types with excess manufacturability margin. Therefore, step (e) of modifying portions (i.e. pattern types, specific to extra margin, paragraph [0046]) of the layout (i.e. design is compacted, paragraph [0046]) is performed despite their existing no violation of any of the plurality of design rules; and this is evidenced by paragraph [0046] where Kroyan discloses "extra manufacturability margin" where no design tolerances [i.e. rules] are violated because all of Kroyan's rules are minimal tolerance rules as described in paragraph [0021].

42. Applicant asserts that Kroyan fails to teach: providing a graphical representation indicating structures demonstrating poor manufacturability/extra manufacturability margin. Examiner disagrees with this assertion.

Examiner points out that Kroyan teaches: providing a graphical representation indicating structures demonstrating poor manufacturability/extra manufacturability margin (i.e. geometrical configuration of the layout, pg 6, paragraph [0087]).

### *Conclusion*

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suchin Parihar
Examiner
AU 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER